

U.S. Department of Commerce, Patent and Trademark Office (PTO Form 1449 modified)					Docket No. ROC920010293US1	Serial No. UNKNOWN	
<b>LIST OF PATENTS AND PUBLICATIONS CITED BY APPLICANT</b>					Applicant BERGLUND ET AL.	Confirmation No.: UNKNOWN	
(Use several sheets if necessary)					Filing Date Herewith	Group UNKNOWN	
		Examiner UNKNOWN					
<b>U.S. Patent Documents</b>							
*Examiner Initial		Document Number	Issue Date	Applicant(s) Name	Class	Subclass	Filing Date Appropriated
	A1	5,434,775	07-18-1995	Sims et al.	364	403	11-04-1993
	A2	5,913,034	06-15-1999	Malcolm	395	200.53	08-27-1996
	A3	6,023,699	02-08-2000	Knoblock et al.	707	10	03-25-1997
	A4	6,029,199	02-22-2000	Allen et al.	709	224	08-16-1996
	A5	6,052,722	04-18-2000	Taghadoss	709	223	03-07-1997
	A6	6,169,987	01-02-2001	Knoblock et al.	707	10	03-25-1997
	A7						
	A8						
<b>Foreign Patent Documents</b>							
*Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation
							YES
	B1	JP8320816	12/03/1996	Japan			<input type="checkbox"/> X
	B2	GB2346463A	05-04-2000	UK			X <input type="checkbox"/>
<b>OTHER ART</b>							
*Examiner Initial		Including Author, Title, Date, Pertinent Pages, Etc.					
	C1	DMTF; Network Management and Administration, Winston Bumpus, April 3, 2001					
	C2	IButton™ OVERVIEW, Table of Contents, Preface, pp. 1-151					
	C3	Utilizing the World's Last Expensive Network Topology, Mike Willey, VP Paragon Innovations, Inc.; Embedded Systems Conference West 2001, Class No. 546, pp. 1-39					
	C4	Dallas Semiconductor, Application Note 27, Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor iButton™ Products , 11-08-99, pp. 1-16					
	C5	Dallas Semiconductor, Application Note 74, Reading and Writing iButtons via Serial Interfaces, 02-08-00, pp. 1-39					
	C6	Dallas Semiconductor; DS1820, 1-Wire™ Digital Thermometer, 030598, pp. 1-27					
	C7	Dallas Semiconductor; DS2409, MicroLan Coupler, 102199, pp. 1-18					
	C8	Dallas Semiconductor; DS2433, 4k-Bit 1-Wire™ EEPROM, 062299, pp. 1-19					
	C9	Dallas Semiconductor; DS2450, 1-Wire™ Quad A/D Converter, 012401, pp. 1-24					
Examiner				Date Considered			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

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<b>U.S. Patent Documents</b>								
*Examiner Initial		Document Number	Issue Date	Applicant(s) Name	Class	Subclass	Filing Date If Appropriate	
	A1							
	A2							
	A3							
	A4							
	A5							
	A6							
	A7							
	A8							
<b>Foreign Patent Documents</b>								
*Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation	
							YES	NO
	B1						<input type="checkbox"/>	<input type="checkbox"/>
	B2						<input type="checkbox"/>	<input type="checkbox"/>
	B3						<input type="checkbox"/>	<input type="checkbox"/>
<b>OTHER ART</b>								
*Examiner Initial		Including Author, Title, Date, Pertinent Pages, Etc.						
	C10	Dallas Semiconductor; DS2480B, Serial 1-Wire™ Line Driver with Load Sensor, 101999, pp. 1-30						
	C11	Dallas Semiconductor; DS2502, 1 kbit Add-Only Memory, 102199, pp. 1-22						
	C12	Dallas Semiconductor; DS2502-E64, 1EEE EUI-64 Node Address Chip, 102099, pp. 1-2						
	C13	Dallas Semiconductor; Dallas Semiconductor; DS2890, 1-Wire™ Digital Potentiometer, 061500, pp. 1-27						
	C14	Dallas Semiconductor; DS9502, ESD Protection Diode, 102199, pp.1-3						
	C15	Dallas Semiconductor; DS9503m Protection Diode with Resistors, 102199, pp. 1-3						
	C16	Dallas Semiconductor; Tech Brief No. 1, 1-Wire Net Design Guide, 1/21/01, pp. 1-33						
Examiner		Date Considered						
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:  
Berglund et al.

Serial No.: Unknown

Confirmation No.: Unknown

Filed: Herewith

For: Architecture for Connection  
and Aggregation of  
Components Within a Rack

§§§§§ Group Art Unit: Unknown

§§§§§ Examiner: Unknown

JC668 U.S. PTO  
10/074816  
02/13/02  

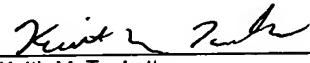

Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

**CERTIFICATE UNDER 37 CFR 1.10**

I hereby certify that this correspondence is being deposited on February 13, 2002 with the United States Postal Service in an envelope as "Express Mail Post Office to Addressee," mailing label No. EV041915927US, addressed to: BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231.

February 13, 2002

  
Keith M. Tackett

**INFORMATION DISCLOSURE STATEMENT**

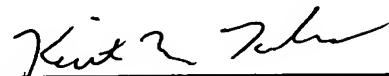
The Applicants, and the Attorney who signs below on the basis of the information supplied by the inventor and the information in his file, submit herewith patents, publications, or other information of which they are aware, which may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

While the information submitted in this Information Disclosure Statement may be material pursuant to 37 CFR § 1.56, it is not intended to constitute an admission that any patent, publication, or other information referred to therein is prior art for this invention unless specifically designated as such.

In accordance with 37 CFR § 1.97, this Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other possibly material information as defined under 37 CFR § 1.56(a) exists.

The patents and/or publications submitted herewith are set forth on the attached Form PTO-1449.

Respectfully submitted,



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